THAT WHICH IS CLAIMED IS:

1. A quantum gate for running quantum algorithms using a certain binary function (*f*) defined on a space having a basis of vectors of *n* qubits, composed of a superposition subsystem carrying out a superposition operation over components of input vectors for generating components of linear superposition vectors referred on a second basis of vectors of *n*+1 qubits, an entanglement subsystem carrying out an entanglement operation over components of said linear superposition vectors for generating components of entanglement vectors, and an interference subsystem carrying out an interference operation over components of said entanglement vectors for generating components of output vectors, said entanglement subsystem comprising

a command circuit (HB14) generating a number (2^n) of logic command signals (Vc1, ..., Vc8) encoding the values of said binary function (*f*) in correspondence of the vectors of the first basis;

an array of multiplexers (I-a), each driven by a respective logic command signal (Vc1, ..., Vc8) and input with a couple of signals (O11, O12; ...; O81, O82) representing components of a linear superposition vector that are referred to vectors of said second basis having the first *n* qubits in common, outputting, for each superposition vector (O11, ..., O82), corresponding signals representing components of an entanglement vector (Vo1, ..., Vo8), each component (Vo1, ..., Vo8) referred to a respective vector of the second basis being

equal to the corresponding component of the

respective superposition vector, if said binary function (f) is null in correspondence of the vector of the first basis constituted by the first n qubits of said respective vector of the second basis, or

the opposite of the corresponding component of the respective superposition vector, if said binary function (f) is non null in correspondence of the vector of the first basis constituted by the first n qubits of said respective vector of the second basis.

2. The quantum gate of claim 1 for running a Grover's quantum algorithm, wherein said interference subsystem comprises

an adder input with voltage signals representing even or odd components of an entanglement vector (Vo1, ..., Vo8) and generating a sum signal (SQ) representing a weighed sum with a scale factor ($1/2^{n-1}$) of said even or odd components;

an array of adders each being input with a respective signal representing an even or odd component, respectively, of an entanglement vector (Vo1, ..., Vo8) and with said sum signal (SQ), generating a signal representing an even or odd component, respectively, of output vector (O1, ..., O8) as the difference between said sum signal (SQ) and said signal representing an even or odd component of an entanglement vector (Vo1, ..., Vo8).

3. The quantum gate of claim 1 for running a Deutsch-Jozsa's quantum algorithm, wherein said interference subsystem comprises an array of adders each being input with signals representing even or odd components of an entanglement vector (Vo1, ..., Vo8)

and generating a signal representing a corresponding even or odd component, respectively, of output vector (O1, ..., O8) as a linear combination of said signals representing even or odd components of an entanglement vector (Vo1, ..., Vo8).

4. The quantum gate of claim 2, further comprising an elaboration subsystem having

an analog/digital converter, input with said signals representing odd or even components of output vector (O1, ..., O8) and converting them in a digital string (D1, ..., D8);

a microprocessor unit input with said digital string (D1, ..., D8), that

calculates a quantity to be minimized (S) associated to said components of output vector (O1, ..., O8),

compares said quantity to be minimized (S) with a certain threshold and stops the Grover's algorithm or commands another iteration whether it (S) is smaller than the threshold or not, respectively,

outputs an output digital string representing components of output vector;

a digital/analog converter input with said output digital string, generating output signals (IN1, ..., IN8) corresponding to odd or even components of output vector;

an array of level shifters, each input with a respective output signal (IN1, ..., IN8), and generating a pair of voltage signals, in a certain voltage range, representing opposite components (O11, O12;

...; O81, O82) of a new superposition vector input to said entanglement subsystem.

5. The quantum gate of claim 4, wherein said analog/digital converter is the commercial device ADC0808;

said microprocessor unit is the commercial device CPLD XC95288XL;

said digital/analog converter is the commercial device AD7228; and

each level shifter is composed of an adder that subtracts a certain voltage (V+) from a respective output signal (IN1, ..., IN8) generating an odd component (O11, O21 ..., O81) of said new superposition vector, and an inverter input with said odd component (O11, O21 ..., O81) generating the corresponding even component (O12, O22 ..., O82).

6. The quantum gate of claim 4, wherein said quantity to be minimized (S) is the Shannon entropy.